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Complete if Known

Application Number	09/880,749
Filing Date	June 12, 2001
First Named Inventor	Draper, Andrew M.
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	015114-053600US

(use as many sheets as necessary)

Sheet	1	of	2
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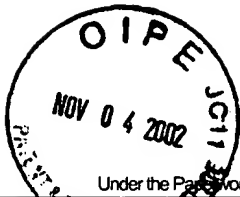
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¹ Applicant's unique citation designation number (optional). ² Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known	
		Application Number	09/880,749
		Filing Date	June 12, 2001
		First Named Inventor	Draper, Andrew M.
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Sheet <u>2</u> of <u>2</u>		Attorney Docket Number	015114-053600US

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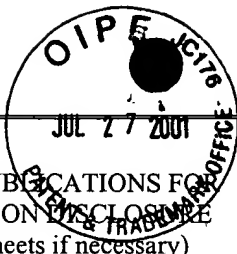
OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			NOV 06 2002
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number(s), publisher, city and/or country where published.	Technology Center 2100
	0011	"AT94K Series Field Programmable System Level Integrated Circuit," Advance Information Brochure of Atmel Corporation, December 1999, 6 pages.	
	0012	"CS2000 Reconfigurable Communications Processor Family Product Brief," Advance Product Information from ChameleonSystems, Inc., 2000, pages 1-8	
	0013	"Motorola Technical Developments," Magazine of Motorola, Inc., Vol. 39, September 1999, pp. i-vii and 77-80.	
	0014	"Triscend E5 Configurable System-on-Chip Family," Product Description from Triscend Corporation, January, 2000 (Version 1.00), pp. i-ii and 1-90.	
	0015	"Wireless Base Station Design Using Reconfigurable Communications Processors," Wireless Base Station White paper from ChameleonSystems, Inc., 2000, pages 1-8.	
	0016	AITKEN, R.C., and AGARWAL, V.K., "A Diagnosis Method Using Pseudo-Random Vectors Without Intermediate Signatures," Proc. of Int. Conf. on Computer-Aided Design (ICCAD), IEEE pp. 574-577 (1989).	
	0017	GHOSH-DASTIDAR, J., and TOUBA, N.A., "A Rapid and Scalable Diagnosis Scheme for BIST Environments With a Large Number of Scan Chains," Proc. of IEEE VLSI Test Symposium, pp. 79-85 (2000).	
	0018	GHOSH-DASTIDAR, J., DAS, D., and TOUBA, N.A., "Fault Diagnosis in Scan-Based BIST using Both Time and Space Information," Proc. of International Test. Conf., IEEE, pp. 95-102 (1999).	
	0019	MC ANNEY, M.G. and SAVIR, J., "There is Information in Faulty Signatures," Proc. of International Test Conf., IEEE, pp. 630-636 (1987).	

Examiner Signature		Date Considered	2/25/2004
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PA 3260057 v1



#4

FORM PTO-1449 (Modified)	Attorney Docket No.: 015114-053600US	Application No.: 09/880,749
LIST OF PATENTS AND PUBLICATIONS FOR DISCLOSURE	Applicant: Andrew Draper	
APPLICANT'S INFORMATION STATEMENT (Use several sheets if necessary)	Filing Date: June 12, 2001	Group: Unassigned 2133

Reference Designation **U.S. PATENT DOCUMENTS** Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
AA	4,488,259	Dec. 11, 1984	Mercy	364	900	
AB	4,710,927	Dec. 1, 1987	Miller	371	15	
AC	5,412,260	May 2, 1995	Tsui et al.	326	39	
AD	6,097,211	Aug. 1, 2000	Couts-Martin et al.	326	40	
AE						

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)
AF						
AG						
AH						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AI	Altera "APEX 20K Programmable Logic Device Family Data Sheet", May 1999	RECEIVED JUN 14 2002 Technology Center 2100
AJ	Altera "FLEX 10K Embedded Programmable Logic Family Data Sheet", May 1999	
AK	Altera "FLEX 8000 Programmable Logic Device Family Data Sheet", May 1999	
AL	Altera "MAX 7000 Programmable Logic Device Family Data Sheet", May 1999	
AM	Altera "IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices" August 1999, Application Note 39	

EXAMINER	DATE CONSIDERED 2/25/04
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